

## **Multispectral HDVIP Focal Plane Arrays\***

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### **Abstract**

The High-Density Vertically Interconnected Photodiode (HDVIP<sup>TM</sup>) architecture developed at Texas Instruments is now the basis of staring focal plane arrays fabricated by RTIS' FPA Business unit. The architecture has been demonstrated to produce high performance, large area scanning and staring arrays, including the world's first true long-wave ( $>10\text{ }\mu\text{m}$  cutoff) 480x640 staring array. In this paper we report on extending the monocolour HDVIP architecture to multispectral arrays capable of simultaneous detection of 2 or more spectral bands.

### **1.0 Introduction**

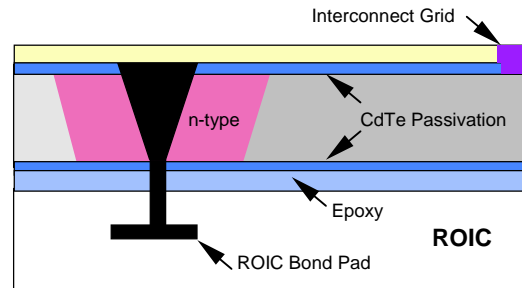
IRFPAs that simultaneously detect in two or more spectral bands may have application in a number of emerging scenarios. Heretofore, all architectures for these devices have required the use of indium bumps to connect the detector diodes to the silicon readout circuit (ROIC). For some time, the FPA Business of Raytheon Systems Company has been developing the HDVIP architecture for monocolour IRFPAs (Figure 1). This architecture differs from others in two important respects: (1) It uses reactive ion etching and ion implantation to form a planar array of diodes. Consequently the etching of mesas to define the individual array pixels, which is required with grown junction approaches, and the subsequent need to passivate these non-planar features is absent. (2) The HDVIP architecture epoxies the detector material directly to the ROIC and uses vertically formed interconnects through vias (i.e., small holes formed in the detector material) to contact the ROIC.

The fabrication process for monocolour arrays is straightforward. A thin (5 – 10  $\mu\text{m}$ ) piece of p-type, copper doped MCT that has been passivated with CdTe on both sides is epoxied to the array area of an ROIC. Vias are cut through the MCT by reactive ion etching (RIE) down to the ROIC bond pads. The RIE, along with ion implantation into the walls of the via and subsequent an-

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nealing, produce the n-type region of the diode. Metal is deposited into these vias and patterned, forming the contacts between the ROIC bond pads and the n-type region of the MCT diodes. A metal interconnect grid is also deposited and patterned onto the top of the array. This grid makes contact to the p-type part of the diode at the corners of the pixel. These contacts insure that there is no voltage drop across the MCT due to optical currents, which would cause problems with diode debiasing effects. Finally, an antireflection coating is deposited onto the top of the array.



**Figure 1.** Schematic cross-section of a HDVIP pixel.

It has been obvious to us for some time that a successful approach for us to multispectral IRFPAs would have to build upon this monocular HDVIP foundation. In particular, it is very important that multispectral devices be able to be fabricated using the same processes and the same processing equipment as the monocular arrays. This commonality means that the multispectral devices will not be “orphans”, but can benefit from all of the process development and support for the monocular arrays.

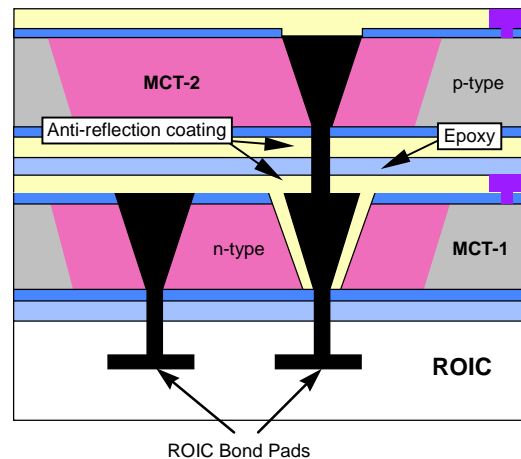
Recently, an extension to the monocular HDVIP architecture to multispectral IRFPAs has been developed within the FPA Business. In addition to preserving all of the benefits of the HDVIP approach to IRFPAs, such as mechanical stability to thermal cycling to cryogenic temperatures, it possesses several advantages in comparison to other approaches:

- (1) The new structure presents fully separated color signals to the ROIC thereby eliminating the need for color subtraction on the ROIC.
- (2) It allows existing monocular ROICs to be used to make high performance demonstration arrays.
- (3) It allows arrays to be fabricated using LPE, as well as MBE, HgCdTe materials.
- (4) Since processing is independent of the HgCdTe cutoffs, cutoffs in a lot may be mixed.

This paper will describe the multispectral HDVIP architecture, and summarize the work that has been done to date to produce the first arrays.

## 2.0 HDVIP Multispectral Architecture

A schematic cross-section through a pixel of a 2-color multispectral array is shown in Figure 2. The fabrication process for this array begins exactly like the monochrome array shown in Figure 1. To form the 2-color array, however, a second via has to be created for each pixel in the bottom MCT layer (right side of the figure). These vias are insulated with ZnS prior to metal deposition. The metal makes contact with the underlying ROIC bond pads. The insulation insures that no electrical contact is made between these metal interconnects (which will later make connection to the n-type regions of the top MCT layer) and the n-type regions of the bottom MCT layer.



**Figure 2.** Cross-section through a 2-color HDVIP pixel.

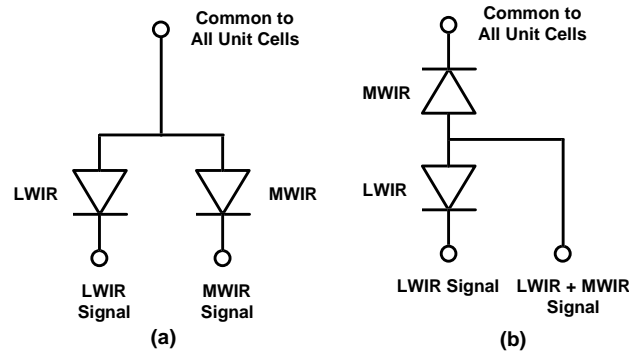
Next, a second piece of thin p-type, copper doped MCT, which has been passivated on both sides with CdTe, is epoxied on top of the structure. This MCT layer differs from the bottom layer in only one respect (other than cutoff): an anti-reflection coating is deposited on it prior to the epoxy bonding. The antireflection coatings on either side of the central epoxy strip are required to efficiently couple IR radiation from the top MCT layer, through the epoxy, and into the bottom layer.

Vias are cut through this top MCT layer over the insulating vias in the bottom layer, exposing the underlying metal. RIE and ion implantation into the walls of the vias and annealing forms the n-type regions of the top diodes. Metal is then deposited and patterned forming the interconnects between the n-type regions of the diodes in the top MCT layer and the underlying metal stubs through the lower insulating vias (which in turn, connect to the ROIC). Finally, the top interconnect grid is deposited to insure contact with the p-type region of the top MCT layer, and a 2-color antireflection coating is applied.

The resulting structure has spatially co-located pixels and it allows simultaneous detection in both wavelength regions, two important requirements of image fusion algorithms. It is important

to note that the diameters of the vias are quite small,  $\sim 7\ \mu\text{m}$ . Even for very small pixel sizes, the fill factor will be quite high.

The electrical structure of the device of Figure 2 is as shown in Figure 3a for a LW/MW implementation. The p-regions of all diodes are in common and connected to the interconnect grids on top of each MCT layer. The n-type regions make contact with the ROIC bond pads. This structure results in complete separation of the photocurrents from each of the two layers. This is in contrast to grown-junction architectures, whose diode electrical structure (shown in Figure 3b) requires that signal subtraction be performed in the ROIC to separate the two color signals. Since the minimum size of a pixel is limited by the space on a ROIC that is needed to accommodate the pixel circuitry, the additional circuitry required to perform the signal subtraction limits the minimum pixel size achievable. This in turn limits the maximum array size that can be fabricated using a given set of design rules.



**Figure 3.** Electrical schematics of detectors in a single pixel that show the inputs to the ROIC. (a). HDVIP. The colors are fully separated. (b) Grown junction detectors such as DLHJ, in which the colors must be separated by the ROIC.

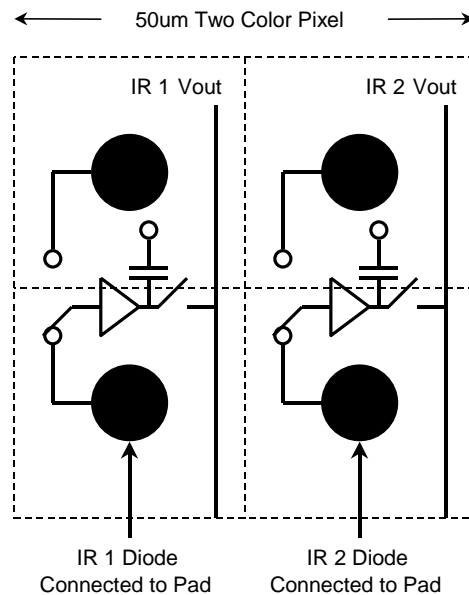
Because the electrical output from the 2-color detectors is the same as for monicolor arrays, the HDVIP architecture allows monicolor ROICs to be used. For example, using the  $480 \times 640$  ROIC developed under the IR/Flexible Manufacturing program, a simultaneously integrating 2-color  $240 \times 320$  array can be fabricated. The interconnection between the diode detectors and the ROIC is shown in Figure 4. The ROIC is designed on a  $25\ \mu\text{m}$  pitch, with one charge integrator shared between two pixels. For the 2-color application, a single pixel will be  $50\ \mu\text{m}$  on a side, spanning 4 of the monicolor pixels. Each of the two diodes in the 2-color pixel will be connected to one of the two charge integrators in the ROIC. This will result in truly simultaneous integration in all pixels and in both colors at the same time.

The performance of this  $240 \times 320$  simultaneously integrating 2-color MW/LW IRFPA has been modeled. For  $f/2$  optics and 120 Hz frame rate, the sensitivities using the existing  $480 \times 640$  ROIC are  $<10\ \text{mK}$  in the LWIR and  $<50\ \text{mK}$  in the MWIR, for the array operating in the simultaneously integrating mode. The MW performance is degraded in this application since the integrating capacitors of the ROIC are selected to accommodate the large charge collected from the LW detec-

tor. In this ROIC, while the integrating capacitors can be selected for optimum LW or MW performance, the selection is made for all cells. For a MW/MW array with the integrator optimized for MW application such as threat warning, the sensitivity is calculated to be <15 mK for both bands.

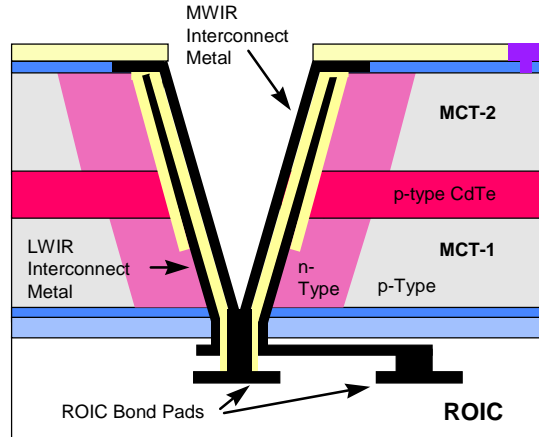
Either LPE or MBE MCT may be used to fabricate the arrays. The thin passivated layers of MCT are currently being produced for all monicolor arrays from LPE. It is a simple matter to substitute MBE MCT into this process. It is also possible to fabricate an array using an all-MBE triple layer as shown in Figure 5. The triple layer consists of two copper doped p-layers having the appropriate cutoffs separated by an arsenic-doped layer of CdTe. The doping in this central layer need only be sufficient to allow current from the p-region of the bottom MCT layer to flow into the top layer, and out through the interconnect grid. The purpose of the insulating layer is to isolate the two n-type regions of the diode. Implantation experiments into semi-insulating MBE CdTe have shown that it remains semi-insulating.

Figure 5 also shows an advanced co-axial interconnect which is feasible by fully exploiting the capabilities of reactive ion etching. Coaxial interconnects promise to allow even smaller pixels to be made.



**Figure 4.** Schematic of the 480x640 ROIC showing interconnects with the 2-color diodes to achieve a 320x640 2-color array.

Extensions to more complex arrays are obvious. For a three color array, a third piece of thin, passivated MCT would be epoxied on the top of the structure of Figure 2, with provision having been made for an additional insulated interconnect through both of the underlying MCT layers. Such an array could also be fabricated using the 480x640 ROIC – a 240x320 3-color array with a 50 µm pitch would result.



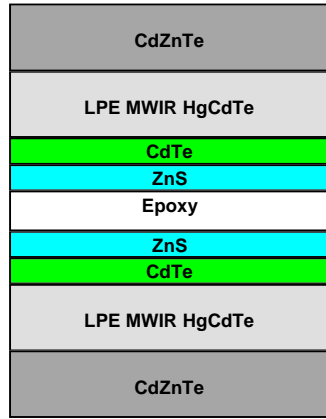
**Figure 5.** HDVIP architecture. In this example, a coaxial interconnect is used, so that one via (i.e., hole) can be used to interconnect the HgCdTe diodes to the ROIC.

### 3.0 Progress

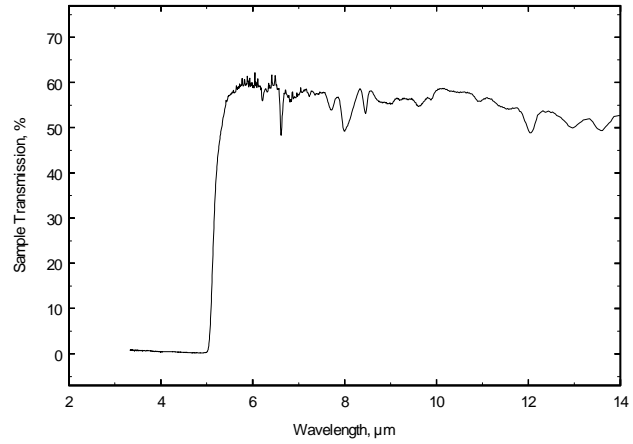
A number of experiments have been undertaken to demonstrate the feasibility of the structure of Figure 2. The first concern was with cracking of the MCT on the ROIC when it was cooled to 77K. Mechanical test structures indicate that cracking is not an issue for total MCT thicknesses of 20  $\mu\text{m}$ .

There was also concern about the optical performance of the 2-color structure of Figure 2. Since a  $\sim 1 \mu\text{m}$  thick epoxy region is required, antireflection coatings on both sides of the MCT layers which contact the epoxy are required to couple radiation into and through the epoxy. In addition there was concern as to whether the epoxy is transparent to IR radiation. To determine the extent to which these concerns limit performance, a test structure was fabricated. It consisted of two pieces of MWIR LPE on CdZnTe substrates. Onto these layers, the antireflection coatings were applied, and they were then epoxied together, forming the structure shown in Figure 6a. The optical transmission was measured at 77K using an FTIR, and the results are shown in Figure 6b. If the LPE layers, epoxy and antireflection coatings had no effect then the transmission should be  $\sim 65\%$ , the theoretical through CdZnTe. In fact, the transmission beyond the MWIR LPE cutoff of 5  $\mu\text{m}$ , the transmission is about 90% of this value, showing that there is no major barrier to the performance of the structure of Figure 2.

The unique processing issues of the 2-color architecture relate to the various vias that are required, and in particular, the technique used to form insulated vias. Insulating vias have now been successfully demonstrated. Figure 7a shows a conventional via through MCT. The via is 6  $\mu\text{m}$  diameter. The dark top layer is photoresist. The via extends through the bonding epoxy to the underlying material, which in this case is silicon. Figure 7b shows an insulating via. The insulation completely coats the inclined MCT surfaces and extends down through the epoxy. The opening, however, extends all the way to the underlying substrate.

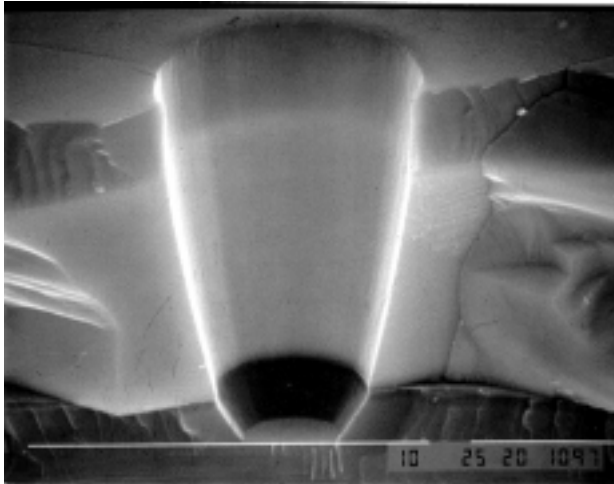


(a)

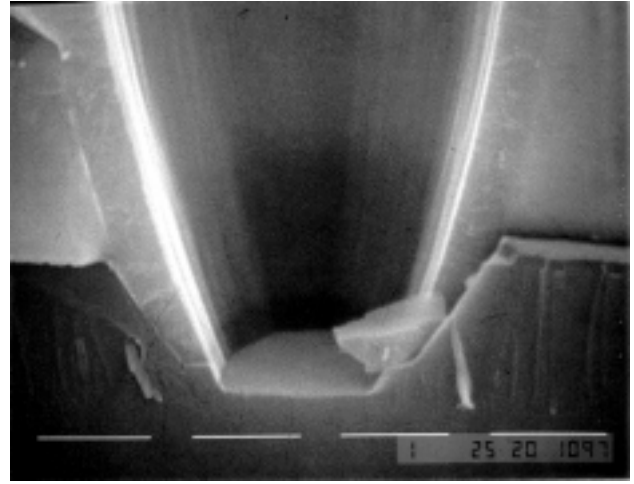


(b)

**Figure 6.** (a) Optical test structure used to evaluate coupling of IR radiation into the bottom MCT layer of Figure 2. (b) IR transmission spectrum at 77K of the structure shown in (a). There is a negligible effect on the transmission in the 6 - 12  $\mu\text{m}$  LWIR region.



(a)

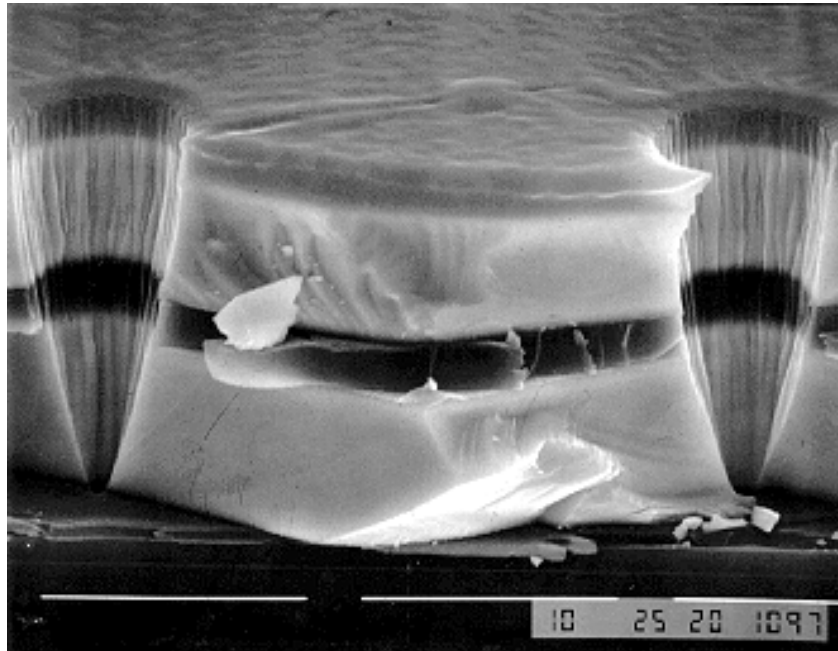


(b)

**Figure 7.** Vias through a single layer of MCT. (a) Standard via. (b) Insulating via. See text for description.

Additional experiments have been conducted in which metal was deposited through similar insulating vias and onto an underlying substrate containing a metal fanout pattern. None of the 600 plus vias were shorted to the MCT. Approximately 150 of the metal interconnects were probed from the top for continuity with the underlying fanout. No opens were found.

We have also taken an initial look at the feasibility of coaxial interconnects. Figure 8 shows vias cut through a double MCT layer. The total thickness of the sandwich is 15  $\mu\text{m}$  and the diameter of the vias at the top is 7  $\mu\text{m}$ .



**Figure 8.** Vias cut through a double layer sandwich of MCT. The layers are (starting from the top) photoresist, MCT epoxy, MCT, epoxy, silicon substrate. The via diameter at the top is 7  $\mu\text{m}$ , and the total sandwich thickness is 15  $\mu\text{m}$ .

As of this writing, the photomasks for the 240x320 2-color FPA have been designed and made, and the first lot of devices is undergoing fabrication. Results from this pathfinder lot should be available later in CY1998.

#### 4.0 Summary

A new approach to 2-color focal plane arrays has been described. It uses the HDVIP architecture to avoid indium bump bonding, and presents several operational advantages. The most critical issues of this approach have been successfully addressed, and the first lot of arrays is now being processed.